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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	5

DATE MAILED: 11/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/721,152	SISKA, CHARLES P.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 Noember 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-21 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: #4. Amendment "A" as received on 9/22/2003.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

5. The abstract of the disclosure is objected to because it is too long. The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. Correction is required. See MPEP § 608.01(b).

6. The disclosure is objected to because of the following informalities: Replace "five16-bit" with --five 16-bit-- on page 10, line 22 (note the space between five and 16).

Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-7, 9-11, 13, and 17-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Hull et al., U.S. Patent No. 5,922,065 (herein referred to as Hull).

9. Referring to claim 1, Hull has taught a method for decoding a first composite packet in a processor, said method comprising the steps of:

a) providing assembly code for each one of a plurality of instructions in a first combination of instructions in said first composite packet. It is inherent that assembly code is provided for packet instructions because assembly code is basic code that an assembler operates upon in order to translate the assembly code into machine code (0s and 1s), which are the only values "understood" by the processor.

b) matching a template in said first composite packet to a known template corresponding to one of a plurality of known syntaxes. See Fig.3 of Hull and note that each packet comprises a template. When a packet is fetched, the template will be matched against all of the possible templates shown in Fig.4. These templates then correspond to known syntaxes, which include information about the types of instructions in the packet and how they are executed. For instance, template 0 corresponds to the MII syntax, i.e., a packet that includes a type of memory instruction and two integer or immediate instructions.

c) matching said one of said plurality of known syntaxes with a resolved packet syntax. From Fig.4, once the template is matched, a resolved packet syntax of the instruction will be determined, i.e., if the template of a packet corresponds to template 0, then the resolved packet index would be a specific type of M-unit instruction, a first I-unit instruction, and a second I-unit instruction.

d) using said resolved packet syntax to determine assembly code associated with execution of said first combination of instructions. If the packet has a template with a value of 0, then assembly code corresponding to the M-unit instruction will be determined, assembly code corresponding to the first I-unit instruction will be determined, and assembly code for the second I-unit instruction will be determined.

e) providing assembly code associated with execution of said first combination of instructions. It is inherent that the assembly code will be executed.

10. Referring to claim 2, Hull has taught a method as described in claim 1. Hull has further taught that said step of matching said one of said plurality of known syntaxes comprises the step of matching each term in said one of said plurality of known syntaxes against a respective term in said resolved packet syntax. For a packet that is assigned a template value of 6, for instance, slot 0 must contain a memory instruction (M-unit), slot 1 must contain a floating-point instruction (F-unit), and slot 2 must contain an integer or immediate instruction (I-unit). Since the processor knows that the first instruction of the packet is a memory instruction, it will find a matching memory type instruction and send it to slot 0. It will then find a matching instruction for slot 1, and so on.

11. Referring to claim 3, Hull has taught a method as described in claim 2. Hull has further taught that said matching step is a direct matching step. It is inherent that the matching step is direct because one item is matched against another term, then these terms are being directly matched.

12. Referring to claim 4, Hull has taught a method as described in claim 1. Hull has further taught that said assembly code associated with execution of said first combination of instructions specifies an issue group for said first combination of instructions. See column 3, line 66, to column 4, line 19. Also, see Fig.4 and note that for template 0, the three sub-instructions form an issue group (referred to as an instruction group in Hull) in that they are contiguous instructions that may be executed concurrently.

13. Referring to claim 5, Hull has taught a method as described in claim 1. Hull has further taught that said assembly code associated with execution of said first combination of instructions specifies a plurality of issue groups for said first combination of instructions. See column 4, lines 43-60. Also, see Fig.4 and note that for template 1, the double lines separating the slot 2 instruction from the slot 1 instruction indicate that the slot 2 instruction is part of a different issue group that that of the slot 0 and slot 1 instructions.

14. Referring to claim 6, Hull has taught a method as described in claim 1. Hull has further taught that said assembly code associated with execution of said first combination of instructions identifies a chained instruction in said first combination of instructions, wherein said chained instruction belongs to an issue group in a second composite packet. See Fig.4, template 1, and column 4, lines 43-67. It should be realized that for template 1, the slot 0 and slot 1 instructions

make up at least part of a first instruction group, and the slot 2 instruction is part of a second instruction group which would include instructions from a subsequent packet (if the stop bit is 0).

15. Referring to claim 7, Hull has taught a method as described in claim 1. Hull has further taught that said assembly code associated with execution of said first combination of instructions identifies a plurality of chained instructions in said first combination of instructions, wherein said plurality of chained instructions belong to respective issue groups in a second composite packet. See Fig.4, template 5, and column 4, lines 43-67. It should be realized that for template 5, the slot 0 instruction makes up at least part of a first instruction group, and the slot 1 and slot 2 instructions are part of a second instruction group, which could include instructions from a subsequent packet (if the stop bit is 0).

16. Referring to claim 9, Hull has taught a method as described in claim 1. Hull has further taught that said known template identifies at least one issue group in said first composite packet. See Fig.4, and note that template 0 specifies an issue group that includes all three of the instructions within the packet. Template 1, on the other hand, specifies that the slot 0 and slot 1 instructions are part of a first instruction group and the slot 2 instruction is part of a second instruction group.

17. Referring to claim 10, Hull has taught a method as described in claim 1. Hull has further taught that said known template identifies a chained instruction in said first combination of instructions, wherein said chained instruction belongs to an issue group in a second composite packet. See Fig.4, template 1, and note that the chained slot 2 instruction would be part of a second instruction group (if the stop bit = 0 for that particular VLIW packet), where the first instruction group comprises at least the slot 0 and slot 1 instructions.

18. Referring to claim 11, Hull has taught a method as described in claim 1. Hull has further taught that said known template identifies a plurality of chained instructions in said first combination of instructions, wherein said plurality of chained instructions belong to respective issue groups in a second composite packet. See Fig.4, template 5, and note that the chained slot 1 and slot 2 instructions would be part of a second instruction group (if the stop bit = 0 for that particular VLIW packet), where the first instruction group comprises at least the slot 0 instruction.

19. Referring to claim 13, Hull has taught a method as described in claim 1. Hull has further taught that said composite packet in said processor consists of 128 bits. See Fig.3.

20. Referring to claim 17, Hull has taught a method as described in claim 1. Hull has further taught that each instruction in said first combination of instructions consists of 41 bits. See Fig.3 and column 3, lines 52-55.

21. Referring to claim 18, Hull has taught a method as described in claim 1. Hull has further taught that said first combination of instructions comprises at least two instructions. See Fig.3 and Fig.4 and note that the VLIW packet format and template allow for as many as three individual instructions to be combined.

22. Referring to claim 19, Hull has taught a method as described in claim 1. Hull has further taught that said first combination of instructions comprises at least one issue group. See Fig.4 and note that template 0 specifies that all three instructions are part of the same issue group while template 1 specifies that the slot 0 and slot 1 instructions are part of a first issue group and the slot 2 instruction is part of a second issue group.

23. Referring to claim 20, Hull has taught a method as described in claim 24. Hull has further taught that said at least one issue group comprises at least one instruction. See column 4, lines 4-7.

24. Referring to claim 21, Hull has taught a method as described in claim 1. Hull has further taught that said template bits consist of at least five bits. See Fig.3 and note that four bits are used to specify a "template" which maps each slot to the appropriate functional unit and specifies instruction group boundaries. In addition, bit 0 of the VLIW packet is for a stop bit, which determines whether an instruction group ends after the last instruction in the bundle (i.e. after the slot 2 instruction). Since all of these bits play a part in controlling how and when the instructions in the VLIW are executed, they can all be considered part of the template. Therefore, the overall template would be 5 bits.

Claim Rejections - 35 USC § 103

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claims 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hull, as applied above.

27. Referring to claim 14, Hull has taught a method as described in claim 1. Hull has not explicitly taught that said composite packet in said processor consists of 256 bits. However, it should be noted that changes in size and/or range, absent evidence of unexpected results from the

change in size and/or change, are generally not given patentable weight or would have been obvious improvements. See In re Rose, 105 USPQ 237 (CCPA 1955). Hull has explicitly taught that a packet is 128 bits but he has further taught that the packet can be any N-bit field. See column 5, lines 59-65. A person of ordinary skill in the art would have recognized that a larger VLIW packet size would allow for larger data (i.e. larger constants and memory addresses), more templates, and more overall instructions, which would result in increase parallelism. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the composite packet in said processor consist of 256 bits.

28. Referring to claim 15, Hull has taught a method as described in claim 1. Hull has not explicitly taught that each instruction in said first combination of instructions consists of 16 bits. However, it should be noted that changes in size and/or range, absent evidence of unexpected results from the change in size and/or change, are generally not given patentable weight or would have been obvious improvements. See In re Rose, 105 USPQ 237 (CCPA 1955). Hull has explicitly taught that each instruction in a VLIW packet is 41 bits. See Fig.3 and column 3, lines 52-55. A person of ordinary skill in the art would have recognized that these instructions could be made smaller in order to reduce the size of the overall program (smaller instructions take up less memory resources than larger instructions). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have each instruction consist of 16 bits.

29. Referring to claim 16, Hull has taught a method as described in claim 1. Hull has not explicitly taught that each instruction in said first combination of instructions consists of 32 bits. However, it should be noted that changes in size and/or range, absent evidence of unexpected results from the change in size and/or change, are generally not given patentable weight or would

have been obvious improvements. See In re Rose, 105 USPQ 237 (CCPA 1955). Hull has explicitly taught that each instruction in a VLIW packet is 41 bits. See Fig.3 and column 3, lines 52-55. A person of ordinary skill in the art would have recognized that these instructions could be made smaller in order to reduce the size of the overall program (smaller instructions take up less memory resources than larger instructions). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have each instruction consist of 32 bits.

30. Claims 8 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hull, as applied above, in view of Gupta et al., U.S. Patent No. 6,457,173 (herein referred to as Gupta).

31. Referring to claim 8, Hull has taught a method as described in claim 1. Hull has not explicitly taught that said plurality of known syntaxes are arranged as a plurality of first level nodes in a tree structure. However, Gupta has taught such a tree structure with first level nodes representing syntaxes. See Fig.2, components 134 and 136, and column 12, lines 1-3. These nodes represent the possible instruction combinations or syntaxes. Gupta has further disclosed that this system may simplify the decoding logic. See column 21, lines 11-14. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Hull such that Hull includes first-level syntax nodes, as taught by Gupta.

32. Referring to claim 12, Hull has taught a method as described in claim 3. Hull has not explicitly taught that said plurality of known syntaxes are arranged as a plurality of first level nodes in a tree structure and said direct matching step comprises matching a term in said resolved packet syntax with a term in a syntax of one of said plurality of first level nodes. However, Gupta has taught such a tree structure with first level nodes representing syntaxes. See

Fig.2, components 134 and 136, and column 12, lines 1-3. These templates are associated with syntaxes which are then matched to a matching resolved packet syntax. For instance, in order to determine which type of resolved packet syntax (138, 140, 142, etc.) the current packet corresponds to, each term of the packet would have to be matched to the terms of the resolved packet syntaxes 138, 140, 142, etc.. Gupta has further disclosed that this system may simplify the decoding logic. See column 21, lines 11-14. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Hull such that Hull includes a plurality of first level syntax nodes in a tree structure and said direct matching step comprises matching a term in said resolved packet syntax with a term in a syntax of one of said plurality of first level nodes.

Conclusion

33. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Petrov, Code Compaction and Parallelization for VLIW/DSP Chip Architectures, June 1999, has taught how combinable instructions in a VLIW packet break down into assembly language code.

Aditya et al., Automatic Design of VLIW and EPIC Instruction Formats, April 2000, has taught how an instruction is disassembled (decoded) based on a template.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (703) 305-7811. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

DJH
David J. Huisman
November 6, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
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